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Applicant : Nihon Denki K. K.

Title : ENTIRELY DIVIDING WAVE CIRCUIT

(57)[ABSTRACT]

[PROBLEM]

A conventional entirely dividing wave circuit processes a digital signal assuming that an effective bit length of a digital signal is constant, so that it is not possible to realize the reduction of electric power consumption in accordance with the number of channels.

[SOLUTION]

An analog portion 1 converts the frequency of an input frequency multiple signal, decomposes a real axis and an imaginary axis of the input frequency multiple signal and further, converts the input frequency multiple signal into digital signals 7a and 7b. A sub filter portion 2 shifts a bit of the digital signals 7a and 7b in accordance with the number of channels in use. As a result, the sub filter portion 2 comprises a bit length reduction circuit 8 for inserting zero in an undefined lower bit, memories 10a and 10b, multipliers 12a and 12b, a multiplication output correcting circuit 14 for setting a lower bit to zero within a range where quantization error is allowed, adders 15a and 15b, delay circuits 16a and

16b and registers 17a and 17b. A FFT portion 3 converts the signal into a signal on a time axis by FFT calculation to output time division multiple signals 24a and 24b.

[0022]

However, if lower 2 to 3 bits are simply set to zero, the quantization error is only increased, so that a system specification is not capable of being satisfied. Therefore, according to this embodiment, amplitude variable means (illustration thereof is omitted in FIG. 1) for increasing the amplitude of the input frequency multiple signal in proportion to the number of channels in use is provided on the input side of the analog portion 1. Further, by setting the lower 2 to 3 bits of the output digital signals of the A/D converters 6a and 6b to zero, the quantization bit length to be processed in actual is decreased as the quantization error of a system request is satisfied. In order to enlarge the signal level in accordance with the number of channels in use without increasing the amount of calculation, the bit length reduction circuit 8 will shift a bit.

FIG. 1 is a block diagram of a first embodiment according to the present invention.

FIG. 1

BLOCK DIAGRAM OF FIRST EMBODIMENT ACCORDING TO PRESENT INVENTION

1: ANALOG PORTION

1F: INPUT

2: SUB FILTER PORTION

3: FFT PORTION

4: MIXER PORTION

8: BIT LENGTH REDUCTION CIRCUIT

10A, 10B: MEMORY MEMORY

11A B: COEFFICIENT COEFFICIENT

14: MULTIPLICATION OUTPUT CORRECTING CIRCUIT

19A, 19B: MEMORY MEMORY

21A, 21B: COEFFICIENT

22: CALCULATION OUTPUT CORRECTING CIRCUIT

23: BUTTERFLY CALCULATION CIRCUIT

24A: ENTIRELY DIVIDING WAVE OUTPUT REAL PORTION

24B: ENTIRELY DIVIDING WAVE OUTPUT IMAGINARY PORTION

25: CONTROL SIGNAL